Please amend the application as follows:

In the Specification:

On page 5, in the second paragraph, please delete the paragraph and insert the following::

-- In the recent U.S. Patent Application number 09/975,630, filed on 10/12/2001 (Taylor R. Efland "Circuit Structure Integrating the Power Distribution Functions of Circuits and Leadframes into the Chip Surface") [(Efland, TI-31678)], an integrated circuit (IC) chip is described, which is mounted on a leadframe and has a network of power distribution lines deposited on the surface of the chip so that these lines are located over active components of the IC. The lines are connected vertically by metal-filled vias to selected active IC components below the lines, and also by conductors to segments of the leadframe. The present invention is related to this disclosure.--

A1

On page 11, in the Section titled "Brief Description of the Drawings", please delete the section and insert the following:

--BRIEF DESCRIPTION OF THE DRAWINGS

A2

FIG. 1 is a simplified perspective and cross sectional view of a power distribution line over an integrated circuit (IC) fabricated in a semiconductor chip attached to a leadframe mount pad, with an electrical conductor connecting to a leadframe segment, according to an embodiment of the invention.

FIG. 2 is a simplified perspective and cross sectional view of a portion of a power distribution line, with connecting member attached, according to a preferred embodiment of the invention.

FIG. 3 is a schematic top view of an IC indicating the positioning of contact pads according to known technology.

FIG. 4 illustrates schematically the positioning of contact pads, with emphasis on morphing a plurality of power supply contact pads into a power distribution line, according to an embodiment of the invention.

FIG. 5A is a schematic and simplified top view of a portion of an IC chip, schematically indicating electrical power connection in prior art, and resulting electrical resistance in current flow.

FIG. 5B is a schematic and simplified top view of a portion of an IC chip, schematically indicating electrical power connection according to the invention, and resulting electrical resistance in current flow.

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FIG. 6 is a schematic diagram of individualized power distribution lines deposited over an active IC for lowering electrical parasitics.

FIG. 7 is a simplified perspective and cross sectional view of a power distribution line over an integrated circuit (IC) fabricated in a semiconductor chip with a solder ball mounted to the distribution line through an opening in a solder mask layer.

FIG. 8 is a simplified perspective and cross sectional view of a power distribution line over an integrated circuit (IC) fabricated in a semiconductor chip with a ribbon connecting the distribution line to a leadframe segment. --

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On page 12, in the first paragraph, please delete the paragraph and insert the following:

A3

-- The present invention is related to U.S. Patent Applications # 08/959,410, filed on 10-28-1997, # 09/611,623, filed on 07-07-2000 (Shen et al., "Integrated Circuit with Bonding Layer over Active Circuitry"), # 60/221,051, filed on 07-27-2000 (Efland et al., "Integrated Power Circuits with Distributed Bonding and Current Flow"), and U.S. Patent Application number 09/975,630, filed on 10/12/2001 (Taylor R. Efland, "Circuit Structure Integrating the Power Distribution Functions of Circuits and Leadframes into the Chip Surface"), which are herewith incorporated by reference.--

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On page 17, in the first paragraph, please delete the paragraph and insert the following:

A4

-- If outermost layer 165 is selected so that it is solderable, a solder ball (700 in Figure 7) can be attached to it by standard reflow techniques. However, it was